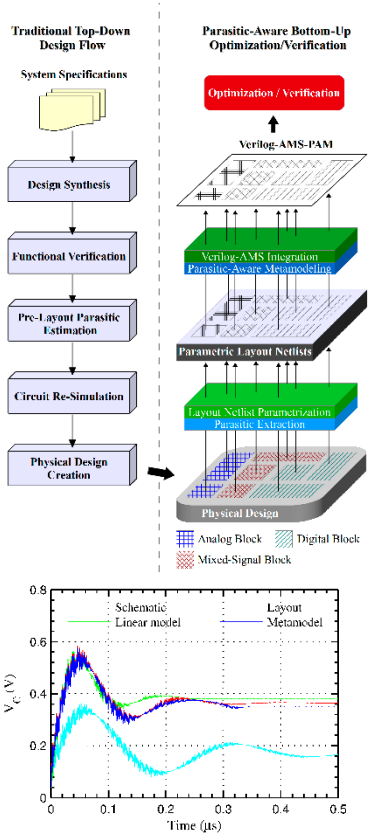
Professor Elias Kougianos

Department of Electrical Engineering

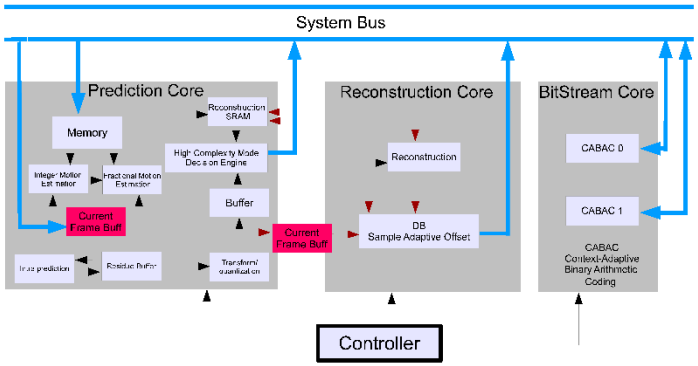
Analog/Mixed-Signal VLSI design and simulation, VLSI architectures for multimedia, Hardware security for the Internet of Things (IoT)

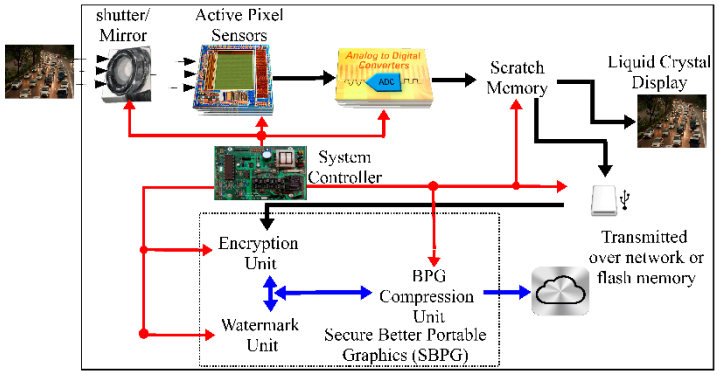
Research Group: Federal, State, Air Force and Industrial Funding; Co-advising 6 Ph.D. and 8 M.S. students

Parasitic-aware Metamodeling Design Flow (US Patent 9,026,964)



VLSI Multimedia Architectures for the IoT





Parasitic-Aware Metamodeling

- Real-time design exploration of very large AMS designs
- Metamodel re-use
- 10,000x speedup over traditional simulation with 2% accuracy

VLSI Multimedia Architectures for the IoT

- First-ever hardware architecture for the BPG image format
- Incorporation of safety features at the source
- Targeted towards the IoT

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